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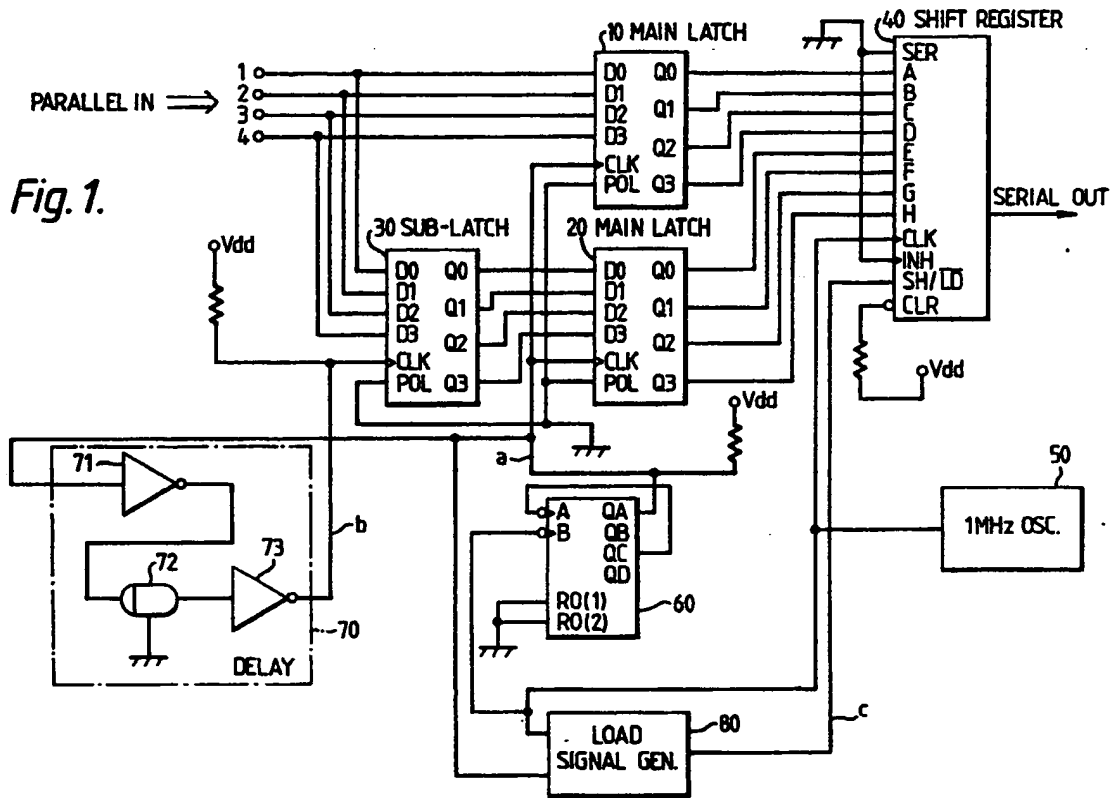
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**JOHN ORCHARD & CO.** Staple Inn Buildings  
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London WC1V 7PZ(GB)(54) **Parallel to serial converter.**

(57) A parallel to serial converter for converting  $n$  ( $n$  being an integer) bit parallel data streams into a serial data stream including first latch means responsive to a first timing pulse for latching the  $n$  bit parallel data streams to produce first  $n$  bit parallel data streams,  $m$  ( $m$  being an integer) second latch means responsive to  $m$  second timing pulses for latching the  $n$  bit parallel data streams to produce  $m$  sets of second  $n$  bit parallel data streams, third latch means responsive to the first timing pulse for latching the  $m$  sets of second  $n$  bit parallel data streams to produce  $m$  sets of third  $n$  bit parallel data streams, shift register means coupled to the first and third latch means and responsive to the first  $n$  bit

parallel data streams and the  $m$  sets of third  $n$  bit parallel data streams and a load pulse for registering  $(m+1) \times n$  bit data from the first  $n$  and  $m$  sets of third  $n$  parallel data streams and for shifting the  $(m+1) \times n$  bit data in response to a shift pulse and timing generating means for generating the first timing pulse,  $m$  second timing pulses, the load pulse, and the shift pulse, the first timing pulse having one- $((m+1) \times n)$ th of the clock rate of the shift clock pulse, each of the  $m$  second timing pulses being delayed by one- $m$ th of a period of the first timing pulse, and the load pulse being timed with the first timing pulse.

**EP 0 397 358 A1**

Fig. 1.



## PARALLEL TO SERIAL CONVERTER

### BACKGROUND OF THE INVENTION

This invention relates to an improvement for a parallel/serial converter which converts parallel signal sequence into a serial signal sequence.

The parallel/serial converter of this type has been used for an interface which converts parallel data from a computer or a communication system to serial data and a multiplexer which multiplexes a plurality of data sequences from plural channels.

A prior art parallel/serial converter comprises a parallel input/serial output shift register and a holding register connected to the parallel input side of the shift register as a buffer store means. (See, for example, pages 4-9 of "Technical Aspects of Data Communication" (in Japanese) published by CQ Publishing Company, on April 20, 1980). The holding register loads and stores  $n$ -bit ( $n$  is an integer) parallel input digital data with a load input, and then the shift register receives the stored data in parallel from the holding register to shift  $n$ -bit serial signal on a bit by bit basis with a shift clock signal which has a higher rate than the input digital data. When the shift register has shifted out the  $n$ -bit serial data, it receives the next  $n$ -bit parallel outputs from the holding register and then converts them to serial data. If the signal rate of the parallel input signal sequence increases, the store means should receive and store each of the parallel input signals at a rate proportionally higher. Therefore, the prior art parallel/serial converter can not operate at the signal rate beyond the capacity of the operational frequency of the holding register and latch circuit.

### SUMMARY OF THE INVENTION

It is an object of this invention to provide a parallel/serial converter which permit operation at a higher bit rate despite the use of components usable at a reduced bit rate.

The parallel/serial converter according to this invention converts  $n$  ( $n$  being an integer) bit parallel data streams into a serial data stream.

The parallel/serial converter comprises: first latch means responsive to a first timing pulse for latching the  $n$  bit parallel data streams to produce first  $n$  bit parallel data streams;  $m$  ( $m$  being an integer) second latch means responsive to  $m$  second timing pulses for latching the  $n$  bit parallel data streams to produce  $m$  sets of second  $n$  bit parallel data streams; third latch means responsive to the first timing pulse for latching the  $m$  sets of second  $n$  bit parallel data streams to produce  $m$  sets of third  $n$  bit parallel data streams; shift register

means coupled to the first and third latch means and responsive to the first  $n$  bit parallel data streams and the  $m$  sets of third  $n$  bit parallel data streams and a load pulse for registering  $(m+1) \times n$  bit data from the first  $n$  and  $m$  sets of third  $n$  bit parallel data streams and for shifting the  $(m+1) \times n$  bit data in response to a shift pulse; and timing generating means for generating the first timing pulse,  $m$  second timing pulses, the load pulse, and the shift pulse. The first timing pulse have one- $(m+1) \times n$ th of the clock rate of the shift clock pulse, and each of the  $m$  second timing pulses is delayed by one- $m$ th of a period of the first timing pulse. The load pulse is timed with said first timing pulse.

### BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be better understood from the following detailed description taken in conjunction with the accompanying drawings in which:

FIG. 1 is a block diagram to show the first embodiment of the parallel/serial converter according to this invention;

FIG. 2 is a timing chart to show the operation of the parallel/serial converter shown in FIG. 1;

FIG. 3 is a block diagram to show the second embodiment of this invention; and

FIG. 4 is a timing chart to show the operation of the parallel/serial converter shown in FIG. 3.

### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

As shown in FIG. 1, a parallel/series converter of this invention comprises a first main latch circuit 10 and a sub-latch circuit 30 which alternately latch 4-bit parallel input digital data streams applied at input terminals 1, 2, 3 and 4 at a constant interval, a second latch circuit 20 which latches the parallel output from the sub-latch circuit 30 simultaneously with the first latch circuit 10, and a parallel input/serial output shift register 40 which converts 8-bit parallel outputs from the first and second latch circuits 10, 20 into a serial data stream.

The 4-bit parallel input signal applied to the input terminals 1, 2, 3 and 4 may be parallel data such as characters or mutually different data streams for each of the input terminals. As shown in FIG. 2, 4-bit parallel input signals A1 - A4, B1 - B4, C1 - C4, D1 - D4, and E1 - E4 (Each of Ai, Bi, Ci, Di, Ei ( $i = 1 \sim 4$ ) indicates a 1-bit signal in 4-bit

parallel data) are continuously supplied at input terminals 1, 2, 3 and 4 at every 4  $\mu$ s, and stored alternately in the main latch circuit 10 and the sub-latch circuit 30. The main latch circuit 10 and the sub-latch circuit 30 latch parallel inputs repeatedly at the period (8  $\mu$ s) two times longer than that of the parallel input signals, respectively. The main latch circuit 10 latches and stores the parallel input signals A1 - A4, C1 - C4 and E1 - E4 in every 8  $\mu$ s while the sub-latch circuit 30 latches and stores the parallel input signals B1 - B4 and D1 - D4 in the period of 8  $\mu$ s but with the delay of 4  $\mu$ s from the main latch circuit 10. The parallel input signals which are stored in the sub-latch circuit 30 are further latched by the main latch circuit 20 simultaneously with the main latch circuit 10.

The latching operation of the main latch circuits 10 and 20 and sub-latch circuit 30 is controlled by an oscillator 50, a 1/8 frequency divider 60 and a delay circuit 70. The oscillator 50 generates a clock signal of the frequency of 1 MHz which is divided in frequency by the 1/8 frequency divider 60 to become a main latch signal a of 125 KHz (with the period of 8  $\mu$ s). The main latch signal a is supplied to the main latch circuits 10 and 20 simultaneously. As shown in FIG. 2, the main latch signal a is preset to rise when the parallel input signal level is stable. The main latch signal a is delayed by 4  $\mu$ s by the delay circuit 70 and supplied to the sub-latch circuit 30 as a sub-latch signal b. The delay circuit 70 comprises a delay line 72 which is serially connected between NOT gates 71 and 73 which shape the waveform of the signal.

The main latch circuits 10 and 20 and the sub-latch circuit 30 are made to latch parallel input signals at the rising edges of the main latch signal a and the sub-latch signal b, respectively, and output them to the output terminals Q0 - Q4 until the next latch time. After the parallel signals A1 - A4 are latched and stored by the main latch circuit 10, the main latch circuits 10 and 20 latch parallel signals C1 - C4 and B1 - B4, and further 8  $\mu$ s later, latch parallel signals E1 - E4 and D1 - D4. The 8-bit parallel outputs from the main latch circuits 10 and 20 are respectively applied to the input terminals A - H of the parallel input/serial output shift register 40 and loaded at the shift register 40 with a load signal c which is generated immediately after the rise of the main latch signal a. The load signal c is the pulse signal of negative logic supplied from a load signal generator 80, and turns to low level in synchronization with the rise of the main latch signal a and to high level after the time (1  $\mu$ m) equivalent to one period of the clock signal from the oscillator 50. The shift register 40 loads the parallel output from the main latch circuits 10 and 20 with the rise of load signal c, and shifts out the loaded 8-bit parallel signal bit by bit basis with the

clock signal from the oscillator 50, in the order of the parallel inputs at the input terminals H, G, F, E, D, C, B, and A. Therefore, the parallel signals A1 - A4, B1 - B4 and C1 - C4 are converted into serial signal sequence A4, A3, A2, A1, B4, B3, B2, B1, C4, C3, C2, C1.

As the latching period at the latch circuits 10, 20 and 30 in the aforementioned embodiment is two times higher than the input period of the parallel input signal sequence at the input terminals 1, 2, 3 and 4, the latch circuits 10, 20 and 30 can use ICs of the operational rate of one half of the prior art ICs.

FIG. 3 shows another embodiment of this invention converter in block diagram. In FIG. 3, the parallel/serial converter comprises the first, second and third main latch circuits 11, 12 and 13 and the first and second sub-latch circuits 14, 15 which can use ICs operating at the rate lower than the latch circuits 10, 20 and 30 of the first embodiment, and a parallel input/serial output shift register 41 shifts the 12-bit parallel data fed from the main latch circuits 11, 12 and 13 and converts them to a serial data sequence.

Similarly to the parallel input signals shown in FIG. 2, 4-bit parallel input digital signals A1 - A4, B1 - B4, ... are continuously supplied to input terminals 1, 2, 3 and 4 in every 4  $\mu$ s as shown in FIG. 4. The first latch circuit 11 and the first and second sub-latch circuits 14, 15 are connected to the input terminals 1, 2, 3 and 4. The first main latch circuit 11 latches the first parallel input signals A1 - A4 at the rise of the main latch signal a1 of the period of 12  $\mu$ s. The main latch signal a1 is a clock signal of the period of 12  $\mu$ s which is obtained by dividing the frequency of the clock signal of 1 MHz from the oscillator 50 by 12. Then, the first sub-latch circuit 14 latches parallel input signals B1 - B4 at the rise of a first sub-latch signal b1 which is obtained by delaying the main latch signal a1 by 4  $\mu$ s at the delay circuit 70a. The second sub-latch circuit 15 latches parallel input signals C1 - C4 at the rise of a second sub-latch signal b2 obtained by delaying the first sub-latch signal b1 by 4  $\mu$ s at the delay circuit 70b. The parallel input signals which have been latched at the main latch circuit 11 and sub-latch circuits 14, 15 are stored and outputted until next rises of respective latch signals a1, b1, b2. The 4-bit parallel outputs from the first sub-latch circuit 14 are latched by the third main latch circuit 13 at the rise of the main latch signal a1 while the 4-bit parallel outputs from the second sub-latch circuit 15 are latched by the second latch circuit 12 at the rise of the main latch signal a1.

When the main latch circuit 11 latches parallel input signals A1 - A4, the main latch circuits 12, 13 do not latch any signals because the sub-latch

circuits 14, 15 have not stored the parallel signal respectively. But when the main latch circuit 11 latches parallel input signals D1 - D4, the main latch circuits 12, 13 latch respectively the parallel inputs C1 - C4 and B1 - B4 which have been stored by the sub-latch circuits 15 and 14. Therefore, the main latch circuits 11, 12 and 13 output parallel input signals D1 - D4, C1 - C4, and B1 - B4 to the shift register 41 for the period of 12  $\mu$ s after the main latch circuit 11 has outputted parallel signals A1 - A4.

The shift register 41 loads 12-bit parallel signals from the main latch circuits 11, 12 and 13 at the rise of load signal c1 which is generated immediately after the rise of the main latch signal a1, and shifts them out bit by bit with the clock of 1 MHz from the oscillator. The shift register 41 converts the 12-bit parallel signals into a serial signal in every 12  $\mu$ s. The load signal c1 is a pulse signal of negative logic generated from a load signal generator 81 which is shifted to low level at the rise of the main latch signal a1 and shifted to high level after one period of clocks from the oscillator.

The parallel/serial converter shown in FIG. 3, can use a latch circuit of the lower rate than those used for the converter shown in FIG. 1. For permitting the use of latches operable at a further reduce of bit rate, additional sub-latch circuit and main latch circuit may be connected in parallel between input terminals and a shift register to increase the number of parallel inputs of the shift register as well as to increase the latch period proportionally to the number of the main latch circuits.

Although two to three 4-bit latch circuits are connected in parallel to the main latch circuit in the parallel/serial converters shown in FIGs. 1 and 3, only one latch circuit of 8-bit or 12-bit may be used instead.

As described in detail in the foregoing statement, this invention provides a sub-latch means which latches parallel input signals different from those in the first latch means, and a second main latch which latches the parallel inputs stored in the sub-latch means simultaneously with the first main latch means, and the first and second main latch means supply plural parallel outputs of the rate lower than the original parallel input signals to a parallel input/serial output shift register. Therefore, the operational frequencies of respective latch means are reduced in proportion of the number of the parallel inputs to the shift register, and the main and sub-latch means can use low rate ICs even if the parallel input signals have a higher rate.

## Claims

1. A parallel to serial converter for converting n

(n being an integer) bit parallel data streams into a serial data stream comprising:

first latch means responsive to a first timing pulse for latching said n bit parallel data streams to produce first n bit parallel data streams;

m (m being an integer) second latch means responsive to m second timing pulses for latching said n bit parallel data streams to produce m sets of second n bit parallel data streams;

third latch means responsive to said first timing pulse for latching said m sets of second n bit parallel data streams to produce m sets of third n bit parallel data streams;

shift register means coupled to said first and third latch means and responsive to said first n bit parallel data streams and said m sets of third n bit parallel data streams and a load pulse for registering  $(m+1) \times n$  bit data from said first n and m sets of third n parallel data streams and for shifting said  $(m+1) \times n$  bit data in response to a shift pulse; and timing generating means for generating said first timing pulse, m second timing pulses, said load pulse, and said shift pulse, said first timing pulse having one- $((m+1) \times n)$ th of the clock rate of said shift clock pulse, each of said m second timing pulses being delayed by one-mth of a period of said first timing pulse, and said load pulse being timed with said first timing pulse.

2. A parallel to serial converter for converting n (n being an integer) bit parallel data streams into a serial data stream comprising:

first latch means responsive to a first timing pulse for latching said n bit parallel data streams to produce first n bit parallel data streams;

second latch means responsive to a second timing pulse for latching said n bit parallel data streams to produce second n bit parallel data streams;

third latch means responsive to said first timing pulse for latching said second n bit parallel data streams to produce third n bit parallel data streams;

shift register means coupled to said first and third latch means and responsive to said first n bit parallel data streams and said third n bit parallel data streams and a load pulse for registering  $2 \times n$  bit data from said first n and third n parallel data streams and for shifting said  $2 \times n$  bit data in response to a shift pulse; and

timing generating means for generating said first and second timing pulses said load pulse, and said shift pulse, said first timing pulse having one- $(2 \times n)$ th of the clock rate of said shift clock pulse, said second timing pulse being delayed by one-half of a period of said first timing pulse, and said load pulse being timed with said first timing pulse.

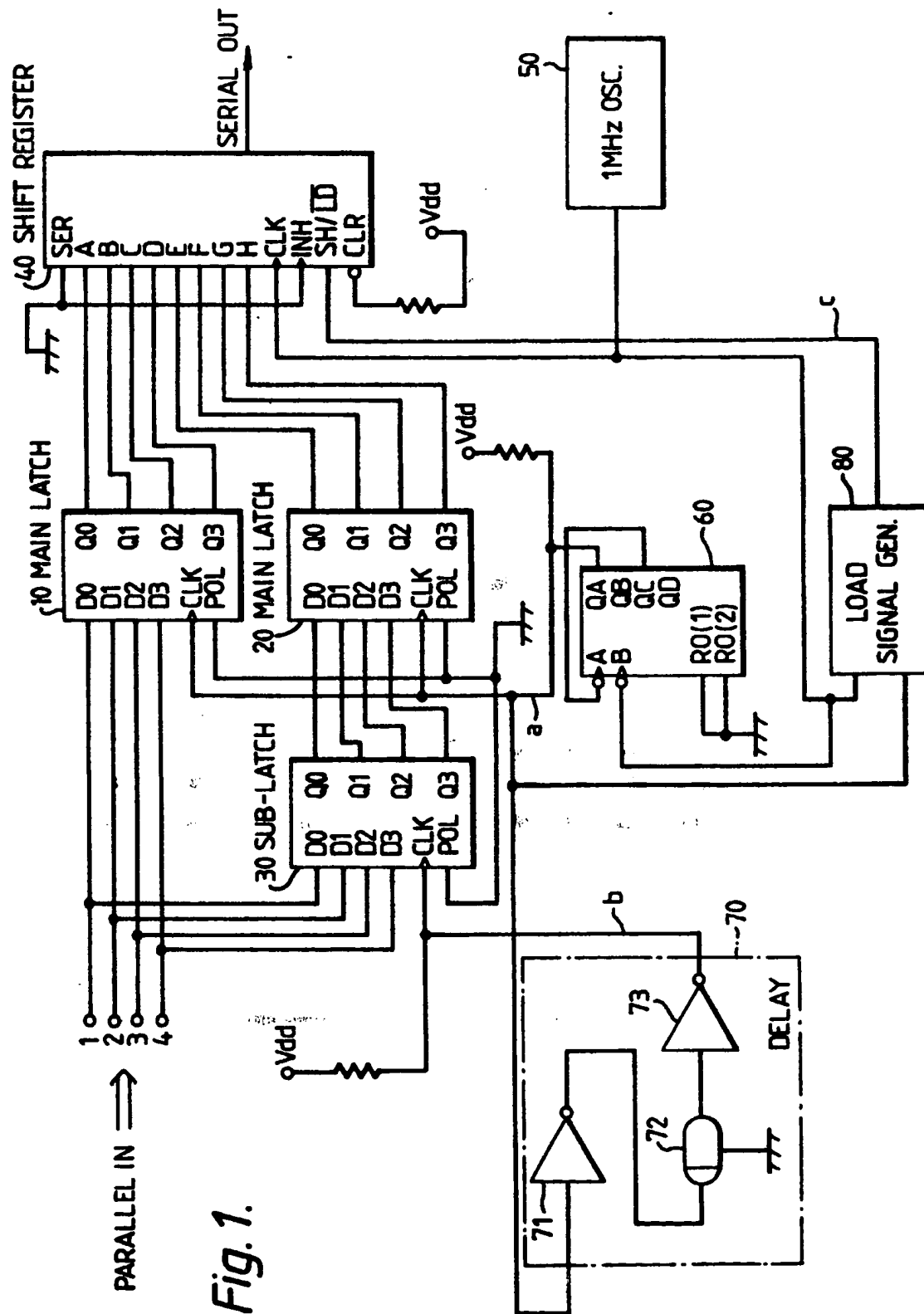
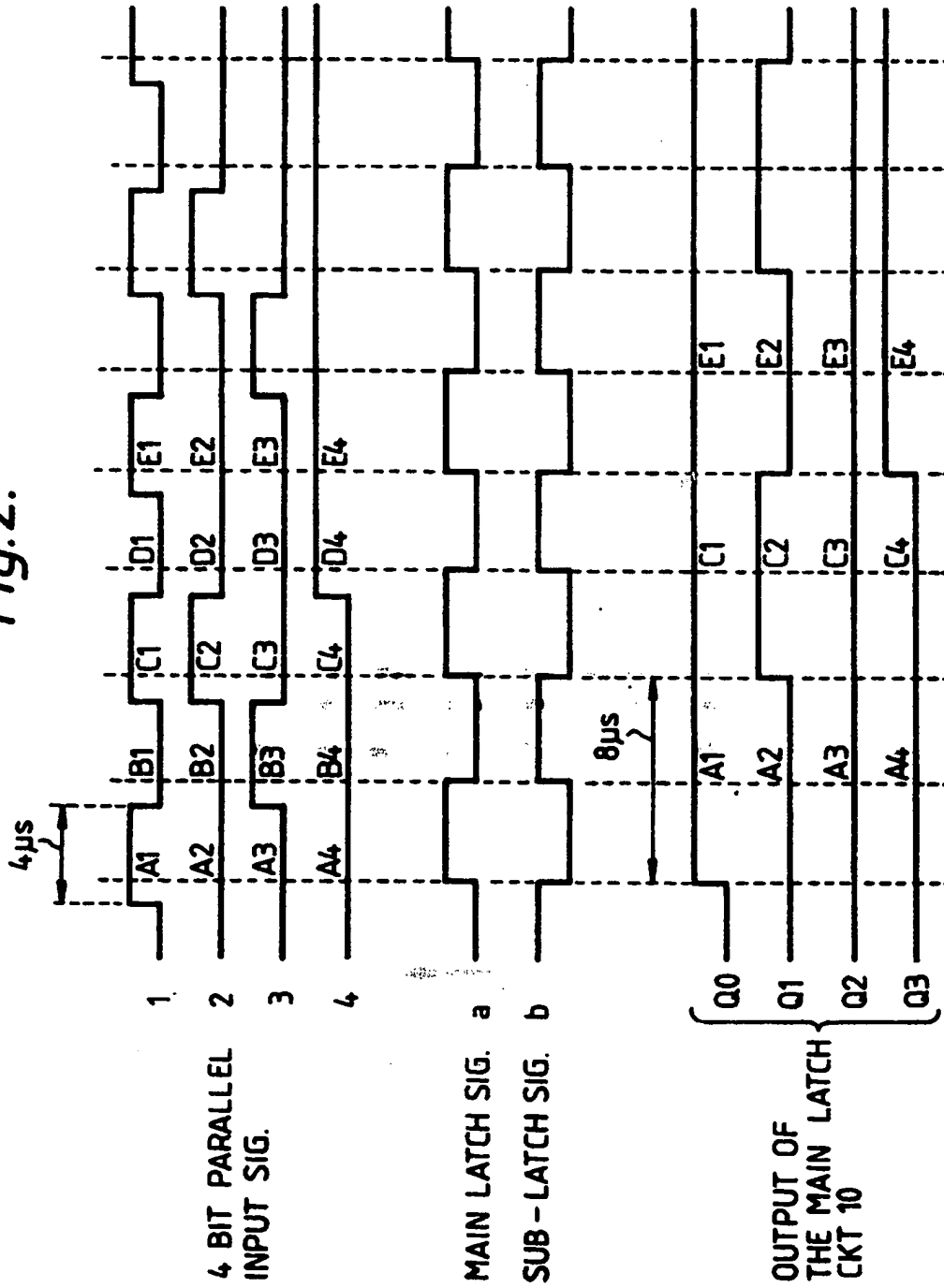


Fig. 2.



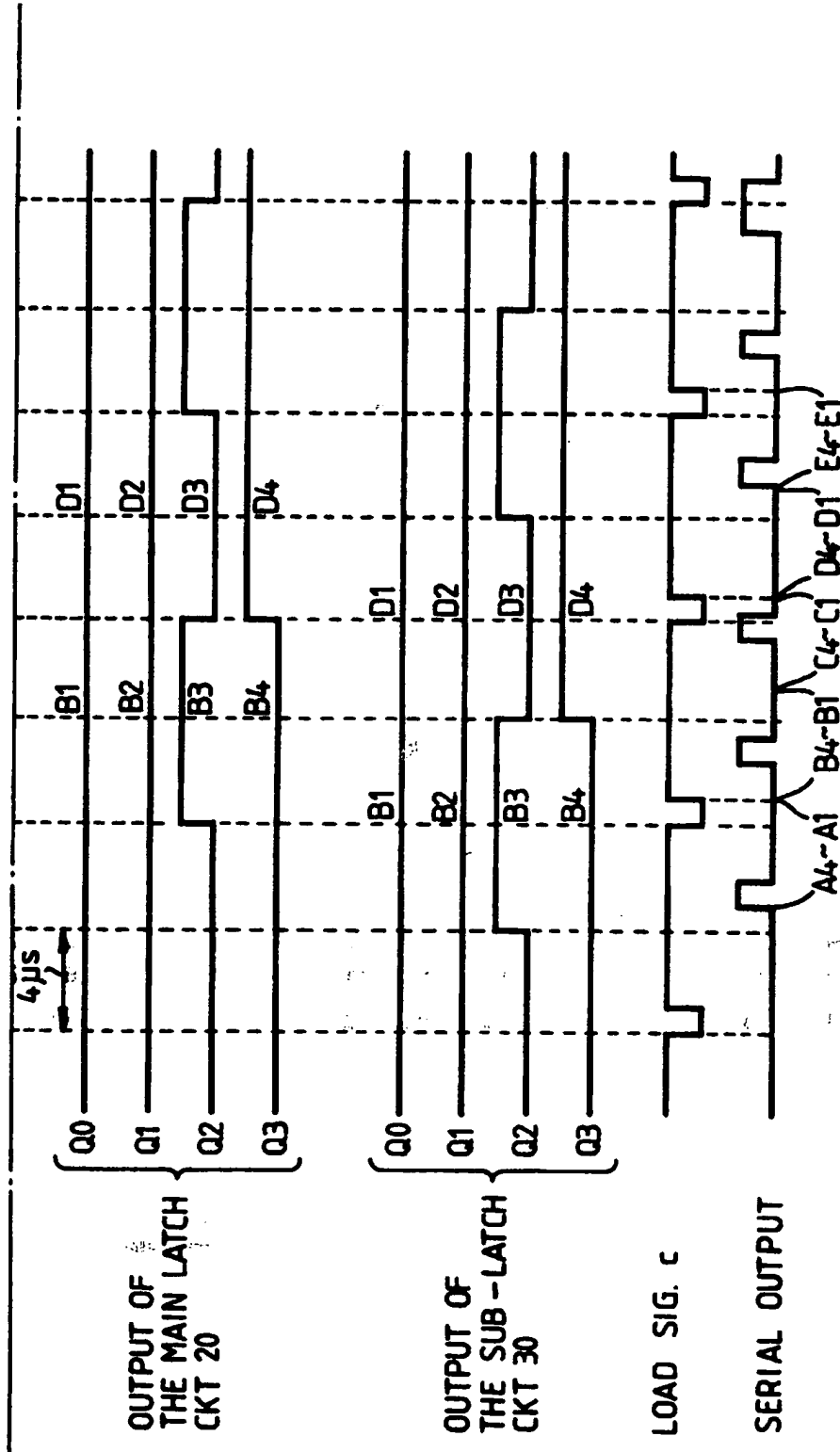


Fig. 2(cont.)



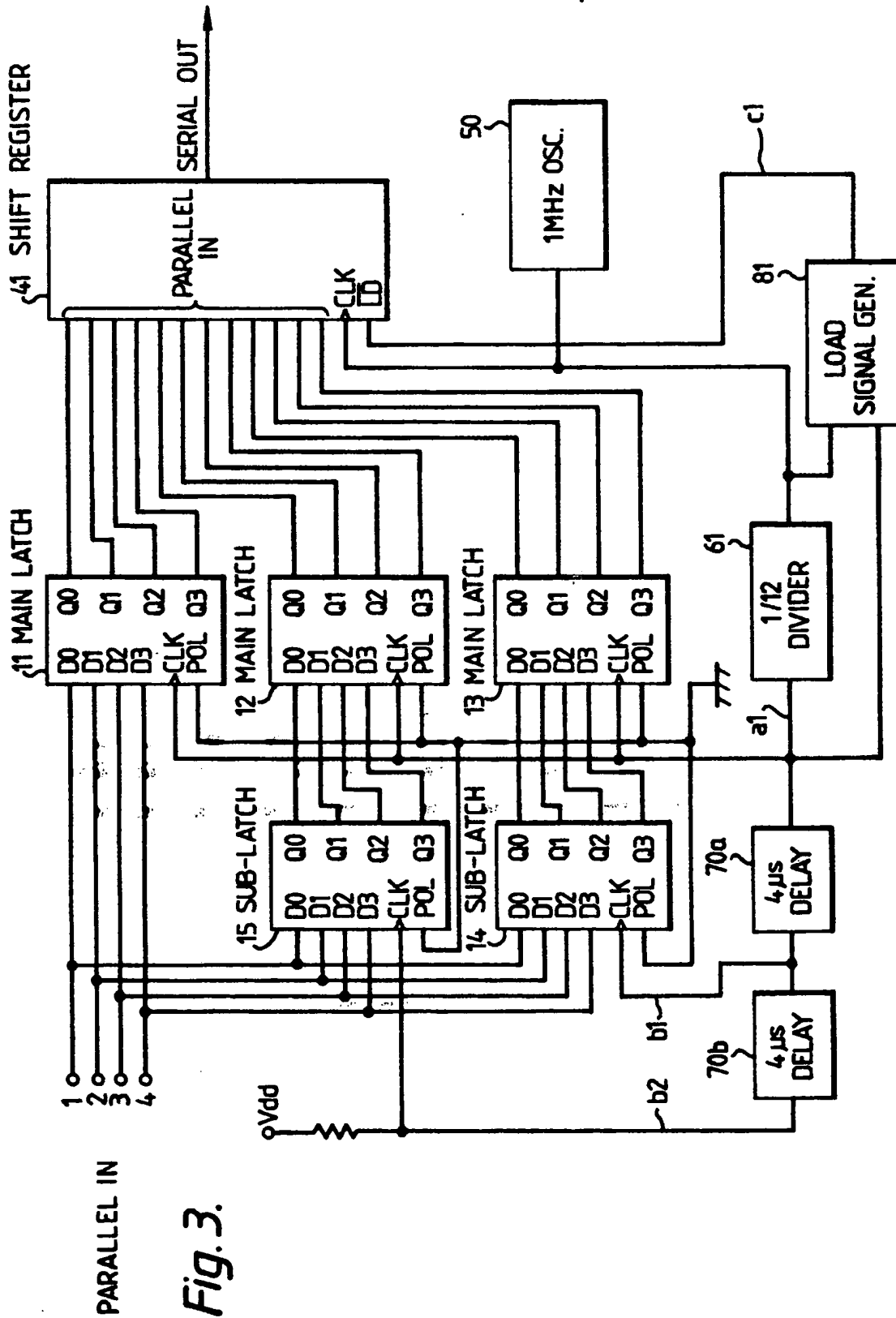
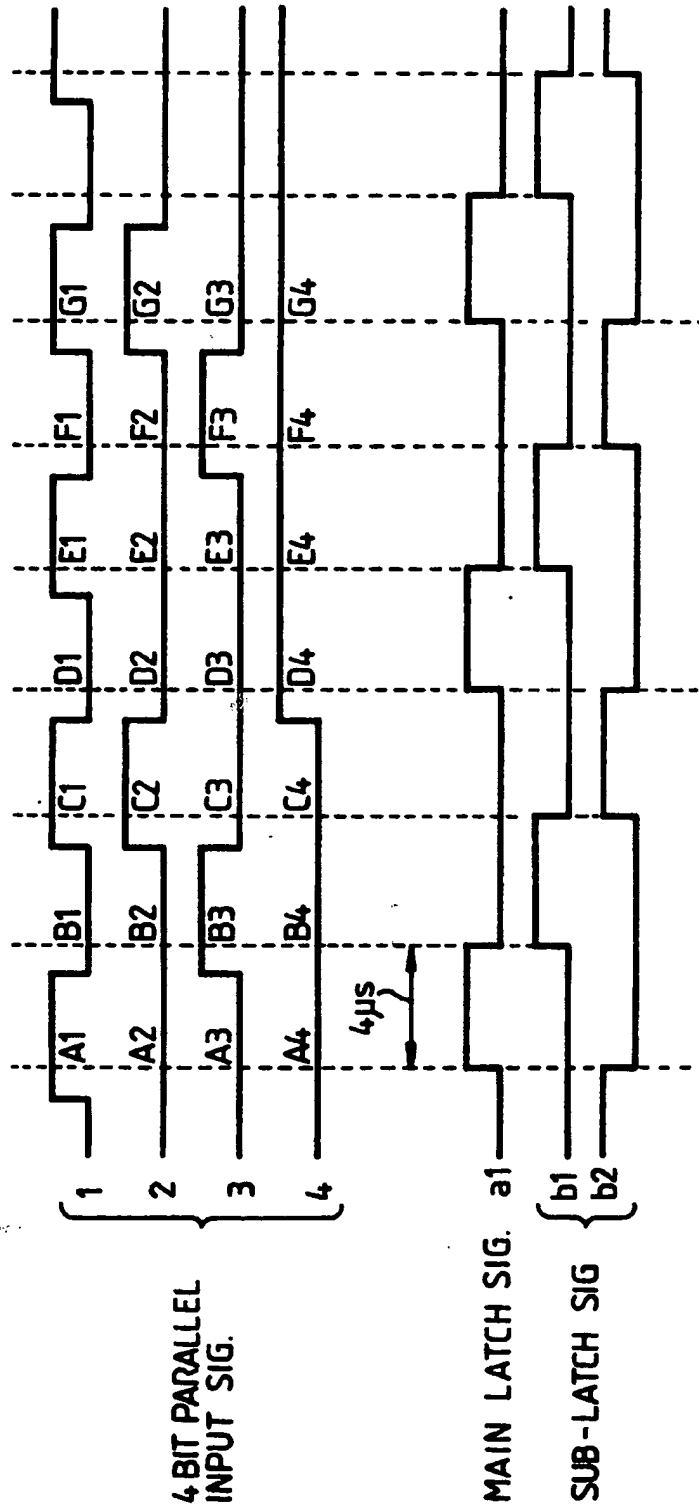


Fig. 4.



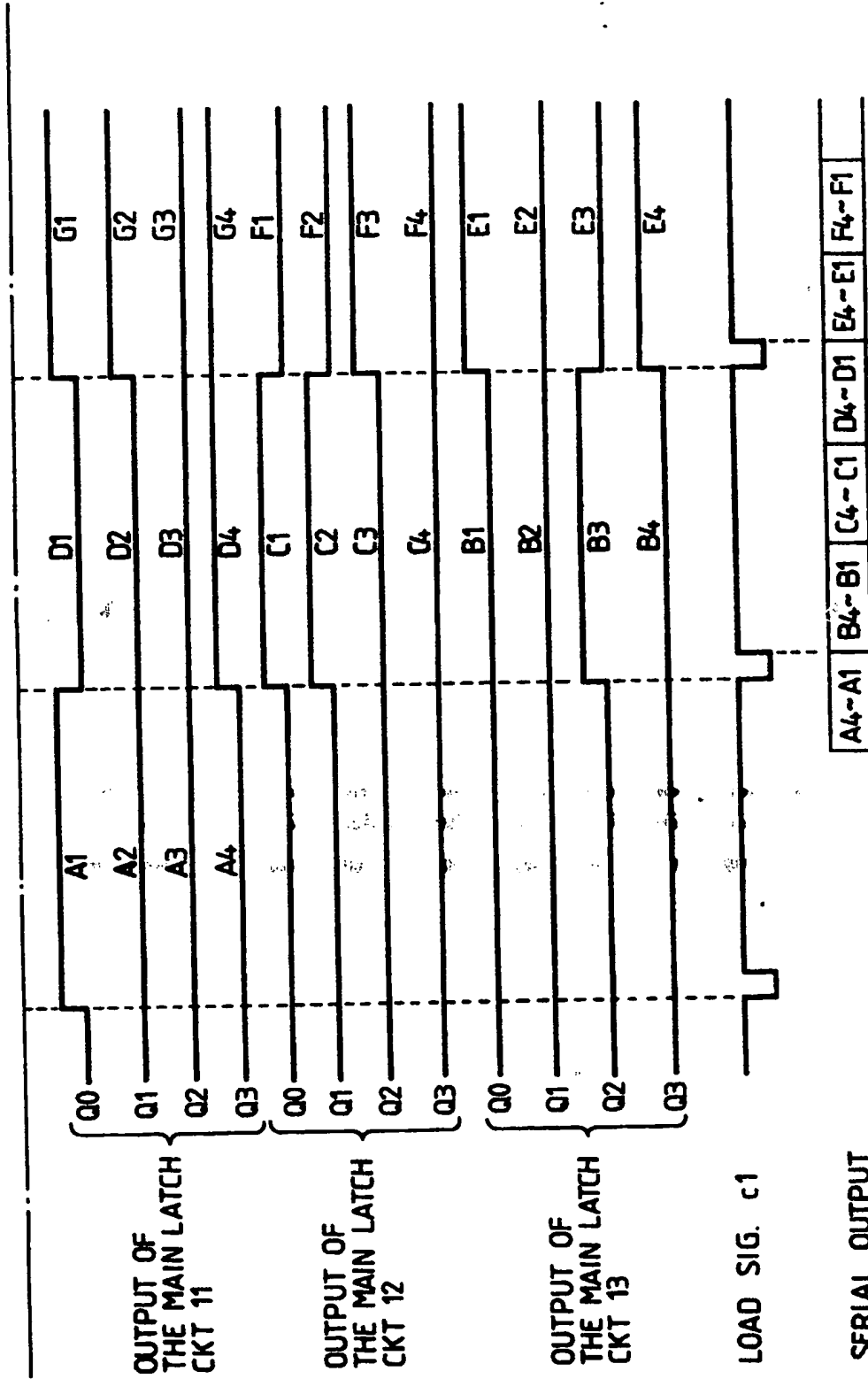


Fig. 4 (cont.)



DOCUMENTS CONSIDERED TO BE RELEVANT			EP 90304595.3
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.)
A	<u>EP - A2/A3 - 0 220 802</u> (NORTHERN TELECOM LIMITED) * Fig. 3; abstract *	1,2	H 03 M 9/00
A	<u>US - A - 4 218 758</u> (ALLEN et al.) * Totality *	1,2	
A	<u>US - A - 4 728 930</u> (GROTE et al.) * Abstract *	1,2	
A	<u>JP - A - 62-233 931</u> (FUJITSU TEN) * Totality * & DERWENT ACCESSION NO. 87-329 913 (47)	1,2	
A	<u>JP - A - 64-73 830</u> (HITACHI) * Totality * & DERWENT ACCESSION NO. 89-126 906 (17)	1,2	
			TECHNICAL FIELDS SEARCHED (Int. Cl.)
			H 03 M 9/00
The present search report has been drawn up for all claims			
Place of search VIENNA		Date of completion of the search 21-08-1990	Examiner BAUMANN
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X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	